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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Timothy A. Rost

Docket No: TI-36595

Serial No: 10/785,648

Conf. No: 3709

Examiner: Long Pham

Art Unit: 2814

Filed: 02/24/2004

For: TRANSISTOR DESIGN AND LAYOUT FOR PERFORMANCE IMPROVEMENT WITH STRAIN

ELECTION

Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 5-2-05.

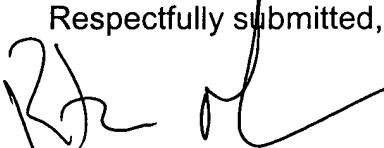
Ann Trent  
Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed April 4, 2005.

Applicant hereby elects to pursue Group I of Claims 9-23, drawn to semiconductor process, without traversing the Examiner's restriction requirement.

Respectfully submitted,

  
Peter K. McLarty  
Attorney for Applicant  
Reg. No. 44,923

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